WHAT IS CLAIMED IS:

1. A floating gate transistor comprising:

a pillar of semiconductor material that extends outwardly from a working surface of a substrate to form a source region, a body region and a drain region of a floating gate transistor;

a floating gate along one side of the pillar; and

a control gate overlaying the floating gate.

2. The floating gate transistor of Claim 1, wherein charges are selectively stored in the floating gate in programming the floating gate transistor.

3. The floating gate transistor of Claim 1, wherein the pillar is formed by etching.

4. The floating gate transistor of Claim 1, wherein an absence or a presence of stored charges on the floating gate determines a conductivity state of the transistor between the source region and the drain region.

5. The floating gate transistor of Claim 1, wherein the substrate is a bulk semiconductor substrate.

6. The floating gate transistor of Claim 1, wherein the substrate is a silicon-on-insulator substrate.

7. The floating gate transistor of Claim 2, wherein hot electron injection is used to program the floating gate transistor.

8. The floating gate transistor of Claim 2, wherein Fowler-Nordheim tunneling is used to program the floating gate transistor.

9. An array of floating gate transistors comprising:

a plurality of semiconductor stacks arranged in rows and in columns, wherein each stack forms source, body, and drain regions of a respective floating gate transistor;

a plurality of floating gates in trenches between the columns of semiconductor stacks, wherein the floating gates are separated from respective sides of the semiconductor stacks by a gate dielectric; and

a plurality of control gates overlaying the respective floating gates and separated from the respective floating gates by an intergate dielectric.

10. The array of Claim 9, wherein etching is used to form the plurality of semiconductor stacks which extend vertically from a substrate.

11. The array of Claim 9, wherein each of the respective floating gate transistors extend outwardly from a substrate with a source region formed proximally to the substrate, a body region above the source region, and a drain region above the body region.

12. The array of Claim 11, wherein two floating gates lie adjacent to each other in each trench between the columns of semiconductor stacks, and one control gate overlays the adjacent floating gates.

13. The array of Claim 11, wherein one floating gate lie in each trench between the columns of semiconductor stacks, and one control gate overlays the floating gate.

14. The array of Claim 11, wherein two floating gates lie adjacent to each other in each trench between the columns of the semiconductor stacks, and two corresponding control gates lie adjacent to each other above the floating gates.

15. The array of Claim 12, wherein the array is a memory cell array with the source regions of common rows electrically connected to be first input selection lines, the control gates electrically connected along the direction of the columns to be second input selection lines, and the drain regions of common columns electrically connected to be output data lines.

16. The array of Claim 13, wherein the array is a logic array with the source regions of a common column electrically coupled to be selection lines during programming of the logic array, the control gates electrically coupled along the direction of the columns to be inputs to the logic array, and the drain regions of a common row electrically coupled to be output lines of the logic array.

17. The array of Claim 14, wherein the array is a field programmable logic array with the source regions of a common column electrically interconnected, the drain regions of a common row electrically interconnected, and the control gates interconnected along the direction of the columns.

18. The array of Claim 15, wherein charges are stored in the floating gates to represent respective data in the memory cell array.

19. The array of Claim 18, wherein hot electron injection is used to selectively place charges in the respective floating gates, thereby programming the respective floating gate transistors.

20. A floating gate transistor that is fabricated upon a substrate, the floating gate transistor comprising:

a first conductivity type semiconductor pillar formed upon the substrate, wherein the pillar has top and side surfaces;

a first source/drain region of a second conductivity type formed in a portion of the pillar that is proximal to an interface between the pillar and the substrate;

a second source/drain region of a second conductivity type formed in a portion of the pillar that is distal to the substrate and separated from the first source/drain region;

a gate dielectric formed on at least a portion of one side surface of the pillar;

a floating gate substantially adjacent to a portion of the side surface of the pillar and separated therefrom by the gate dielectric;

an intergate dielectric formed on a top surface of the floating gate; and

a control gate substantially overlaying the floating gate and insulated therefrom by the intergate dielectric.

21. The floating gate transistor of Claim 20, wherein electrical charges in the floating gate controls electrical conduction between the first source/drain region and the second source/drain region.

22. The floating gate transistor of Claim 20, wherein the floating gate transistor is a data storage element in a programmable memory array with the data represented by charges stored in the respective floating gates.

23. A method for forming an array of vertical transistors with horizontal gate layers, said method comprising:

forming source, body and drain layers on top of one another on a substrate;

etching the source, body and drain layers to form substantially parallel first troughs in a first dimension and substantially parallel second troughs in a second dimension which is substantially orthogonal to the first dimension;

forming floating gates along sidewalls of the second troughs; and

forming control gates on top of the respective floating gates.

24. A method for forming a vertical transistor with horizontal gate layers, said method comprising:

forming source, body and drain layers on top of one another on a substrate;

etching the source, body and drain layers to form substantially parallel first troughs in a first dimension and substantially parallel second troughs in a second dimension which is substantially orthogonal to the first dimension;

depositing dopant layers and a sacrificial gate layer in the second troughs;

heating the partially formed array to form lightly doped source/drain regions in the body layer;

removing at least one of the dopant layers;

replacing the sacrificial gate layer with a floating gate; and

forming a control gate above the floating gate.